ABSTRACT OF THE DISCLOSURE

In a semiconductor integrated circuit device, a command decoder is adapted to receive not only an external command but also an internal command. An ECC controller has a command generator and an address generator. When the command decoder decodes an external entry command, the command generator instructs encoding to an ECC-CODEC circuit and the address generator sequentially produces addresses which are supplied to a memory array. The ECC-CODEC circuit produces check bits for error detection/correction with reference to information data of the memory array. Upon completion of an encoding operation of writing the check bits into a predetermined region of the memory array, the ECC controller delivers an end signal to the command decoder as the internal command to make a super self-refresh control circuit start a super self-refresh operation.